Notice of References Cited	Application/Control No. 09/894,007	Applicant(s)/Patent Under Reexamination FOUGHT ET AL.	
	Examiner John P Trimmings	Art Unit 2133	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-5,646,948	07-1997	Kobayashi et al.	714/719
	B	US-5,805,601	09-1998	Takeda et al.	370/505
	C	US-5,621,739	04-1997	Sine et al.	714/724
	D	US-6,512,707	01-2003	Miura et al.	365/194
	E	US-5,959,487	09-1999	Kawamura, J. Patrick	327/270
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	"Delay Test of Chip I/Os Using LSSD Boundary Scan", Gillis et al., 18-23 October 1998, Test Conference Proceedings 1998, pp 83-90.
	V	"GTLP16616 17-Bit TTL/GTLP Bus Transceiver With Buffered Clock", June 1997, Spec Sheet, Fairchild Semiconductor.
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.